these drawings that the thickness of a semiconductor device of TSOP type can be reduced by arranging two semiconductor chips in the region surrounded by lead frames. In addition, the manufacturing method of the second embodiment employing spot welding to accomplish efficient production is suitable for low cost and mass production of semiconductor devices.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A semiconductor device having:

terminal electrodes located, in plan view, outside a region where semiconductor chips are located;

a lower semiconductor chip overlapping in height with said terminal electrodes;

an upper semiconductor chip located opposite said lower semiconductor chip;

wires connecting said upper and lower semiconductor chips to said terminal electrodes; and

an encapsulating resin encapsulating said upper and lower semiconductor chips and said wires, wherein said encapsulating resin and said terminal electrodes have respective bottom surfaces coplanar with each other.

2. (Amended) The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and coplanar with said terminal electrodes, and wherein said lower semiconductor chip does not overlap, in plan view, said die pad.

3. (Amended) The semiconductor device according to claim 1, wherein said lower semiconductor chip and said encapsulating resin have respective bottom surfaces coplanar with each other and the bottom surface of said lower semiconductor chip is exposed and not covered by said encapsulating resin.

4. (Amended) The semiconductor device according to claim 1, including a die pad supporting said upper semiconductor chip and not coplanar with said terminal

electrodes, and wherein said lower semiconductor chip has a bottom surface encapsulated by said encapsulating resin.

5. (Amended) The semiconductor device according to claim 1, wherein said semiconductor device is a QFN (Quad Flat Non-Lead) Package having said terminal electrodes surrounding said upper and lower semiconductor chips.

6. (Amended) The semiconductor device according to claim 1, wherein said upper and lower semiconductor chips are respectively rectangular in shape, connection terminals of said upper and lower semiconductor chips are arranged along shorter sides of said upper and lower semiconductor chips, opposing each other, and said upper and lower semiconductor chips cross each other, in plan view.

A9 cont

7. (Amended) The semiconductor device according to claim 1, wherein said terminal electrodes are leads located along two opposing sides of said semiconductor device with said upper and lower semiconductor chips therebetween.

8. (Amended) A semiconductor device TSOP (Thin Small Outline) Package having:

upper and lower semiconductor chips arranged between a first lead portion and a second lead portion, respectively, on two opposing sides of said semiconductor device, in plan view;

a first die pad integrated with and not coplanar with said first lead portion and located on one side of a reference plane passing through a central position between a first surface and a second surface of said first and second lead portions; and

a second die pad integrated with and not coplanar with said second lead portion and located on a second side of the reference plane, wherein said lower semiconductor chip is supported by said first die pad and said upper semiconductor chip is supported by said second die pad portion, said upper and lower semiconductor chips are partially overlapping and overlap in height with said first and second lead portions.

9. (Amended) The semiconductor device according to claim 8, including:

a first lead frame connected to said first die pad and located, with said first lead portion, on the first side of said reference plane, and

a second lead frame connected to said first die pad and located, with said second lead portion, on the second side of said reference plane.

10. (Amended) The semiconductor device according to claim 9, wherein

said first die pad portion is L-shaped and includes a first extension extending from an end of said first lead portion toward said second lead portion, and a first opposing portion continuing from said first extension and extending parallel to said first lead portion,

said second die pad portion is arranged, in plan view, opposite said first die pad , is L-shaped, and includes a second extension extending from an end of said second lead portion toward said first lead portion and a second opposing portion continuing from said second extension and extending parallel to said second lead portion,

said first extension and said first opposing portion have bottom surfaces supporting said lower semiconductor chip, and

said second extension and said second opposing portion have upper surfaces supporting said upper semiconductor chip.

11. (Amended) The semiconductor device according to claim 8, wherein said first and second lead portions and said first and second die pads are integrated into a common lead frame, said reference plane passes centrally through the thickness of said lead frame, said first die pad supports said lower semiconductor chip of said partially overlapped upper and lower semiconductor chips, and said second die pad supports said upper semiconductor chip.

12. (Amended) The semiconductor device according to claim 11, including adhesive layers respectively bonding said upper and lower semiconductor chips to said first and second die pads wherein a center of the thickness of said first die pad portion and a center of the thickness of said second die pad portion are spaced from said reference

plane in respective opposite directions, each by a distance equal to the sum of one-half the thickness of said lead frame and one-half the thickness of said adhesive layers bonding said upper and lower semiconductor chips to said first and second die pads.

13. (Amended) A method of manufacturing a semiconductor device comprising:

stacking a first lead frame on a second lead frame, said first lead frame including a first lead portion and a first die pad extending in an L-shape from an end of said first lead portion along a periphery of a region where a lower semiconductor chip is arranged, said second lead frame including a second lead portion and a second die pad opposing said first die pad, in plan view, and extending in an L-shape from an end of said second lead portion along a periphery of a region where an upper semiconductor chip is arranged, said first and second lead portions being opposite each other, in plan view, with said upper and lower semiconductor chips therebetween;

bonding said lower semiconductor chip to said first die pad and bonding said upper semiconductor chip to said second die pad;

welding together said first lead frame and said second lead frame where they overlap;

connecting said upper and lower semiconductor chips to a terminal electrode with a wire;

encapsulating in a resin a region inside of said first and second lead frames that have been welded; and

cutting off a portion, outside said resin, encapsulating said first and second lead portions and said upper and lower semiconductor chips.

14. (Amended) The method of manufacturing a semiconductor device according to claim 13, including combining stacking of said first and second lead frames and bonding of said upper and lower semiconductor chips, and wherein sub steps in the lead frame stacking and sub steps in the semiconductor chip bonding are partially changed in their order.